COLECO INDUSTRIES INC.

COMPUTER LOGIC BOARD

REPAIR GUIDE

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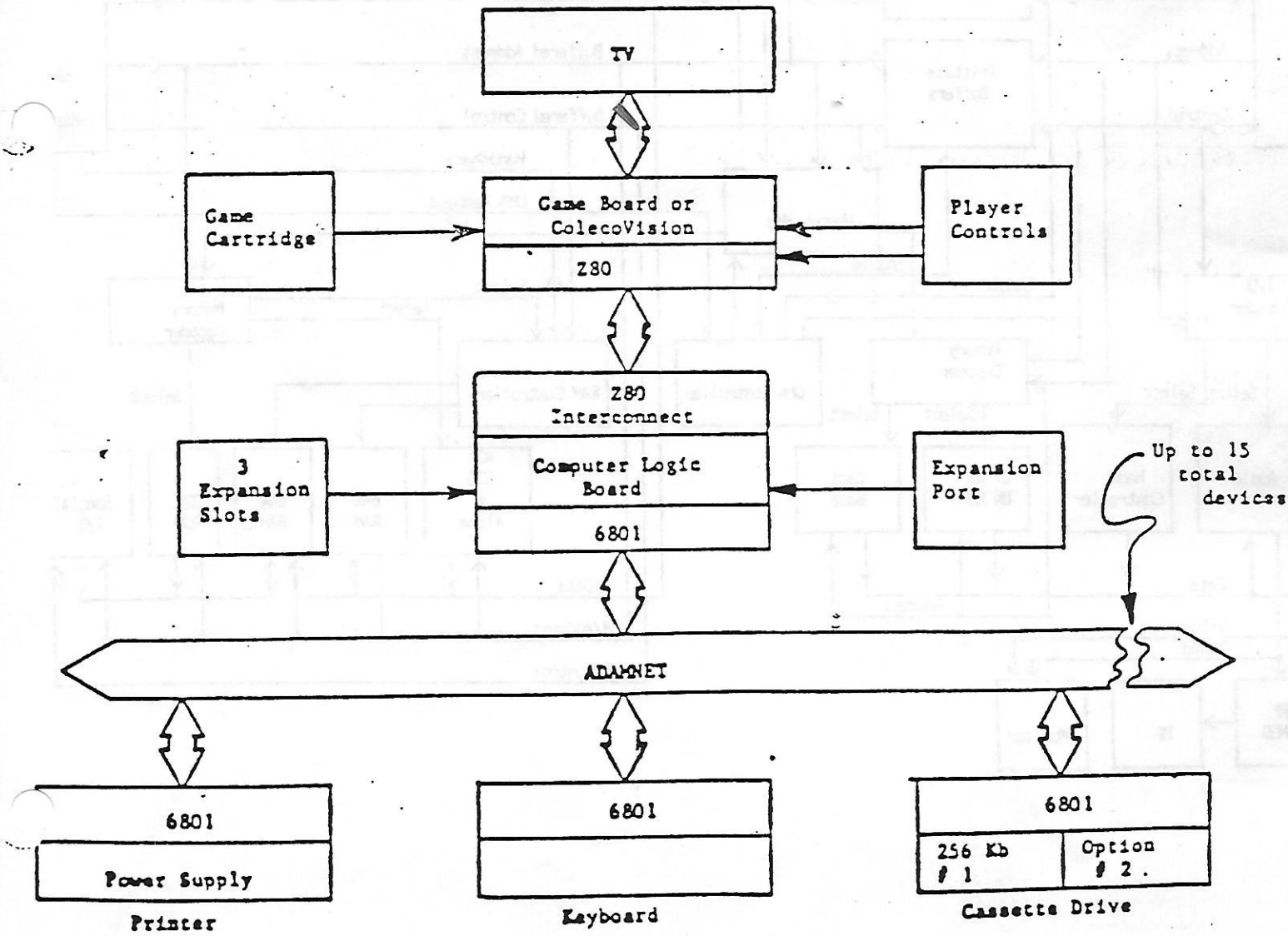
Chapter 1. ADAM COMPUTER SYSTEM BLOCK DIAGRAMS

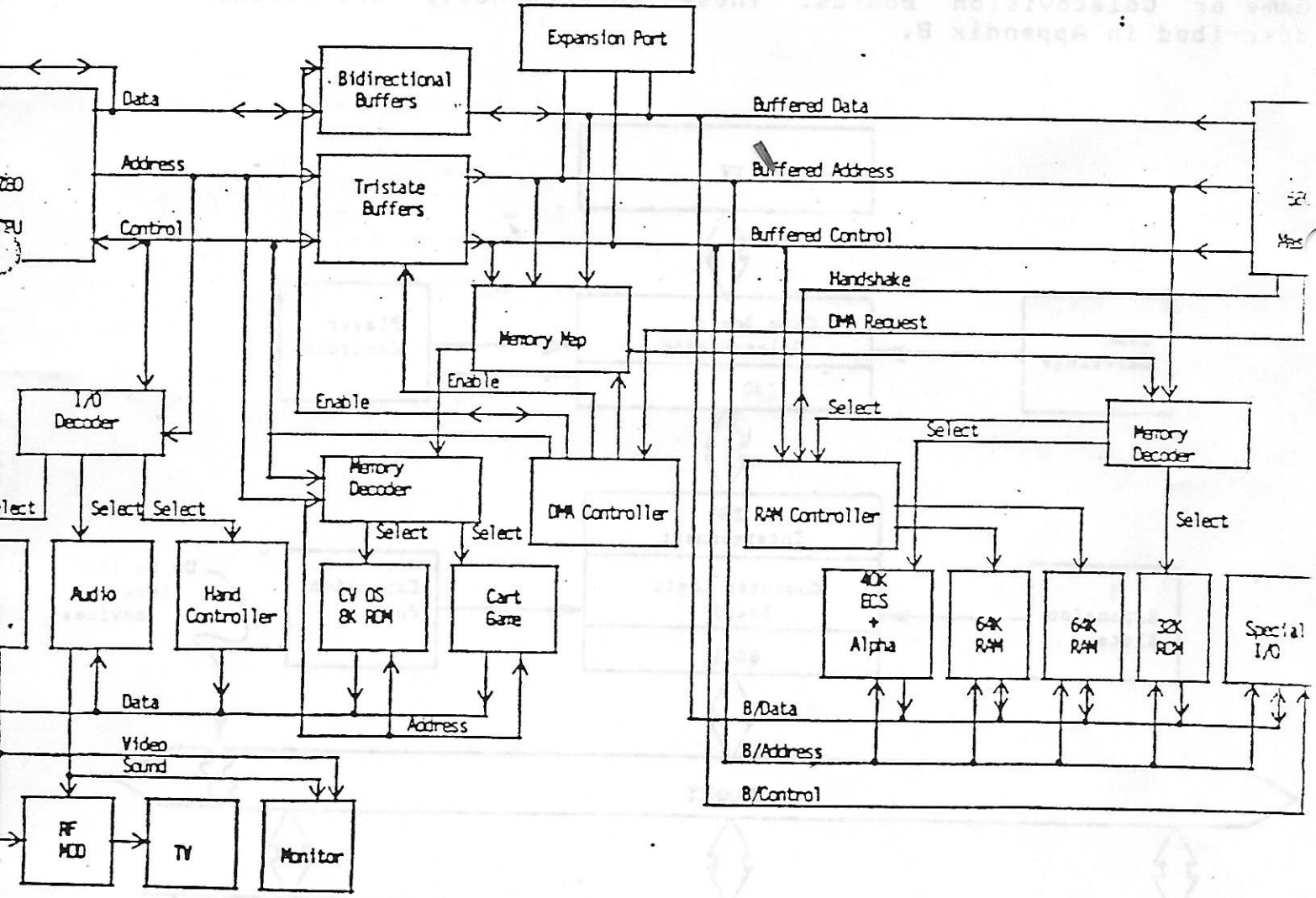
A. Complete System.

The Computer Logic Board, combined with the Delta Game Board or Colecovision and the AdamNet Communications Network make up the main computer system for the Adam Computer. The Computer Logic Board provides the operating system for the word processing and the DRAM used for programming operations. The computer logic board requires two different interconnects to mate with the Delta Game or ColecoVision Boards. These interconnects are further described in Appendix B.



B. Game & Logic Board.

The computer logic board includes 40K Read Only Memory (ROM), 64K Dynamic Random Access Memory (RAM), a Memory Input/Output Controller (MIOC) custom chip, 1K of Static Ram, and two 6801 Processors. The first 6801, referred to as the Master, controls the AdamNet communications network; the second 6801 commands all data drive operations. Each 6801 IC includes an onboard 2048 byte operating system (ROM) and 128 byte scratch pad (RAM).



Chapter 2. HOW TO USE THIS GUIDE

A. Confirm / Verify Problems Described

1. Inspect for physical damage as most probable cause of failures.
   a. Check all connectors, wiring, and components for good connection.
   b. Clean edge fingers and other contact points

2. Check revision level of pc assembly. (See Table, page 6)
   a. 41581D - Delta Computer Logic
   b. 41079D - Gamma Logic

B. Cautions.

1. Handle assemblies and components with care appropriate to avoid damage to static sensitive devices.

   a. Testing must be performed at an ESD protected work station.

      1. Conductive mat/work surface.

      2. Properly grounded operator.

      3. No plastic tools e.g. desoldering tools.

2. Random or non-repeatable errors may occur without proper ground and shield connections in place.

C. Equipment Necessary to perform tests herein described or referenced.

1. System Final Tester
2. Board Level System Tester
3. Known Good Adam Card Set
4. Final Test Cartridge
5. Debug Cartridge

D. Using Customer description of problem and/or previous test results (see Ch 4: Quick Overall Check), use Symptom Index as diagnostic pointer to probable defects and cause.

TABLE 1.

GAMMA & DELTA LOGIC BOARD
REVISION LEVEL IDENTIFICATION CHART

GAMMA		DELTA	
REV LEVEL	Configuration	REV LEVEL	Configuration
		E5	Electronically Equivalent to E4 below
E4	HAS Ferrite Housings	E4	HAS Heatsink and Q-Packs
E3	HAS Heatsink	E3	Does NOT Have C58.
E2	HAS C58	E2	HAS U23
D4	BUSRQ Line from E11 to P1-11	D4	BUSRQ Line from E11 to P1-11
D1	Does NOT Have U8	D1	Does NOT Have U8
D	HAS U8.	D	HAS U8

Chapter 3. SYMPTOM INDEX

Symptoms below are listed in descending order of probability.

SYMPTOM	CAUSE
1. TAPE DRIVE PROBLEMS	
A. Cannot Load Tape (Drive 1)	1. Defective Socket(s) ie. collapsed pins/glue U24, U6, U7.
	2. CR10 Backwards.
	3. Defective U26, U27.
	4. R43 Broken.
	5. Defective U18.
	6. Defective U28.
	7. Data Drive Plugged into wrong port(s).
	8. Defective U29.
	9. Defective U20.
	10. Defective U31.
	11. Defective U6.
	12. C50 shorted to RF Shield.
	13. R62 Missing.

Tape Drive Problems Continued....

B.	Cannot Load Tape (Drive 2)	1. Bent Pins J10, J11.
		2. Defective Socket U24.
		3. Defective U24
		4. Defective U31.

2. VIDEO PROBLEMS

A.	No Video.	1. Defective U7, U28.
		2. J1-60 Open.
		3. J1-E Ribbon cut by shield.
		4. J1 Short to shield.
		5. Cold solder U7.
		6. U23 Pin #15 wire shorted to R70.
B.	Scrambled Video.	1. U7 Bent pin.
		2. Defective U6.
		3. Defective U12.
		4. L9 shorted to shield.
		5. Loose object inside CPU. (Heatsink)
C.	No Video Atari Exp. Mod.	1. Open between P1-32 and J1-32.

3. AUDIO PROBLEMS

A. Atari Expansion Module has no audio.

1. Open between P1-31, J1-31, E31.
2. Dirty gold fingers
3. Open between U7 Pin 36 and P1-35

B. Other Audio Problems.

1. Dirty Finger P1.
2. Bent Pins J1.

4. EXPANSION 64K RAM PROBLEMS

1. U7 Socket, Collapsed Pins/Glue.
2. J5 Pins not thru PCB.
3. R13 Missing Shorted.
4. J5 Missing Pins.
5. Broken Trace J5-3.

5. COMPUTER RESET PROBLEMS

1. Defective socket U6, U20.
2. J1-23, 24 Shorted.
3. Defective U20.
4. Defective U15.

Computer Reset Problems Continued....

5. Reset not seated and sticks on top housing.
6. Defective U14.
7. Defective U13.

6. PRINTER PROBLEMS

A. No Geartrain Advance

1. R32 wrong value. (Should be 33 Ohms)
2. C56 wrong value. (Should be .1uf)
3. Defective socket U7.

7. KEYBOARD PROBLEMS

1. Defective Modular Phone Jack.
2. Broken wires.

8. WORD PROCESSOR PROBLEMS

A. Defective or No W/P Screen.

1. U20, U21, U22 not seated in socket.
2. Defective U7.

Chapter 4. QUICK OVERALL CHECK

A. Check all system interconnections for integrity.

B. Check power supply voltages at all PC Assemblies.

C. Use System Final Tester to highlight functional problems. See Set-up Drawing T-1800 and reference procedure: CPU (System) Cartridge Test (Log# 106.1; Appendix A). Error code information is listed below:

Error Messages:

1. Possible media failure - unsuccessful attempt to access a block on tape during the first pass on the tape test.

2. Fail Aux. Video - Aux. video frequency and amplitude do not meet required limits. Tested at the auxiliary jack located at the rear of the ADAM CPU.

3. Failed controller port # - the state of each pin on the hand controller jacks is changed, sampled, and failed to be at expected level.

4. Controller port interaction - changes at pins of one hand controller port modifies the state of the other port.

5. Read or Write drive fail - unsuccessful attempt to read or write to a tape drive, probably due to inability to access a block.

6. Xfer drive fail - data read from drive under test fails to compare to the data written.

7. Rom Fail - The computed ROM checksums do not compare and the computed values are printed to the screen.

Error Messages Continued....

8. Lower / upper 32K RAM failure - pattern testing on the system RAM failed.

9. Can't sync up with master - communications between the Z80 and the network master 6801 were unsuccessful.

10. Drive 2 or aux. net fail - the signals at the drive two connector were determined to be bad or missing or the auxiliary network connector signals were not present.

Chapter 5. TEST FIXTURES

A. System final test documentation.

1. T-1638 Rev A: System Final Test Assy.
2. T-1132 Rev A: System Test Hardware Sub-Assy.
3. T-1132 Rev A: System Test Hardware Schematic.
4. Log # 106.1: CPU (System Cartridge) Test Procedure.
5. T-1614 Rev B: System Test Interface Harness.
6. T-1619 Rev 0: Interface Harness Wire List.
7. System Test Cartridge Rev 3.1 .
8. Set-Up Drawing T-1800.

B. Board level system test documentation.

1. T-1721 Rev A: Board Level System Test Interconnection Diagram.
2. T-1794 Rev 0: Board Level System Test Interface Harness.
3. T-1797 Rev 0: Interface Harness Wire List.
4. Log #156.0: Logic Board.
5. System Test Cartridge Rev 3.1 .

Chapter 6. SCHEMATICS AND ASSEMBLY DOCUMENTATION

A. Logic Board

1. Delta Logic Assembly: 41581D
2. Gamma Logic Assembly: 41079D
3. Gamma / Delta Schematic: 41843
4. Interconnect Board Assembly: 41571
5. Interconnect Board Schematic: 41840

B. Additional Drawings

1. Delta Game Assembly: 41580
2. Delta Game Schematic: 41844
3. Printer Logic (Compuwriter) Assembly: 41033
4. Computer Logic Schematic: 41218

323-1630
APPENDIX A

TO: M. STRONG PG 1 OF 3
FROM: K.BYRNE
DATE: 7/27/84 ASSEMBLY LEVEL: 541433.5414.8.34EST.
SUBJECT: C.P.U.(SYSTEM CARTRIDGE)TEST PROCEDURE LOG NO.: 108.1

PROCEDURE FOR CONNECTING OF C.P.U. AND TEST MODULE, SLAVE PRINTER AND SLAVE KEYBOARD.

1) CONNECT TEST MODULE TO EXPANSION PORT OF C.P.U.

2) CONNECT KEYBOARD TO SIDE PORT LOCATED ON C.P.U.

3) FOR DELTA C.P.U ONLY. CONNECT TEST MODULE AUX. VIDEO CONNECTOR PORT IN BACK OF C.P.U.

4) CONNECT PRINTER POWER CORD TO RECEPTACLE AND PRINTER ADAM-NET PLUG INTO CORRESPONDING PORT ON C.P.U.

5) CONNECT TEST MODULE AUX.-NET CONNECTOR INTO FRONT PORT OF C.P.U.

6) INSERT TEST CARTRIDGE INTO GAME PORT OF C.P.U.

PROCEDURE	OBSERVATION
1) TURN POWER "ON".	
2) PRESS "COMPUTER" RESET.	2a) "ADAM ELECTRONIC TYPE-WRITER" SCREEN WILL APPEAR ON MONITOR.
3) PRESS "ESCAPE" ON KEYBD.	3a) BLUE WORD PROCESSOR SCREEN WILL APPEAR ON MONITOR
4) TURN POWER "OFF"	

5) CONNECT TEST MODULE HANDCONTROLLER CONNECTORS INTO CORRESPONDING PORTS ON SIDE OF C.P.U., CONNECT TEST MODULE DATA DRVE CONNECTORS INTO PORTS LABELED 2A AND 2B LOCATED ON TOP OF C.P.U.

NOTE: FOR USE WITH A GAMMA SYSTEM, DO NOT PLUG IN TEST MODULE HANDCONTROLLER CONNECTORS.

6) TURN POWER ON	
7) INSERT "BASIC" TAPE IN DATA DRIVE 0.	
8) PRESS "CARTRIDGE" RESET.	8a) TAPE WILL START TO WIND THE MESSAGE " STATION I.D." WILL APPEAR ON MONITOR.
9) TYPE IN YOUR STATION I.D. (FOUR CHARACTERS)	9a) MENU SCREEN WILL APPEAR.
10) CHOOSE #2	10a) MESSAGE "ADAM OR GAMMA?" WILL APPEAR ON MONITOR.

PROCEDURE	OBSERVATION
11) TYPE A IF TESTING AN ADAM C.P.U. TYPE E IF TESTING A GAMMA C.P.U. (EXPANSION MOD. # 3).	11a) WORDS "TEST IN PROGRESS" WILL APPEAR ON THE MONITOR. CHECK FOR ALTERNATING COLORS OF WORDS.

NOTE: AT THIS TIME THE OPERATOR DOES NOT HAVE TO CONTINUOUSLY MONITOR TEST FOR APPROX. 2 1/2 MINUTES. DURING THIS TIME ANOTHER TEST STATION CAN BE SET UP FOLLOWING SET-UP DIRECTIONS OF PREVIOUS PAGE. CHECK UNITS FOR COSMETIC DEFECTS.

11b) AT THE END OF 2 1/2 MIN. THE FOLLOWING WILL APPEAR ON MONITOR IF SYSTEM IS GOOD, COLOR BARS AS FOLLOWS: WHITE
GREY
LIGHT YELLOW
DARK YELLOW
CYAN (BLUE)
LIGHT GREEN
MEDIUM GREEN
DARK GREEN
VIOLET
LIGHT RED
MEDIUM RED
DARK RED
LIGHT BLUE
DARK BLUE

THEN AUDIO TONES WILL BE HEARD FOLLOWED BY A "CROSS-" A GRID PATTERN WILL THEN APPEAR ON SCREEN, CHECK FOR UNIFORMATY OF GRID PATTERN. A SEQUENCE OF MUSICAL NOTES WILL BE HEARD FOLLOWED BY A PROMPT MESSAGE TO "TYPE IN YOUR INITIALS"ON A BACKGROUND OF WHITE. PRESS "RETURN".

NOTE: TYPE IN INITIALS WHEN WHITE SCREEN APPEARS ONLY. TEST WILL RECYCLE UNTIL OPERATOR TYPES IN INITIALS.

11c) IF SYSTEM HAS FAILED SCREEN WILL FLASH RED AND WHITE WITH AUDIO TONE

11d) IF UNIT PASSES STEP 11C THE MESSAGE "PASSED MANUFACTURING TEST" WILL APPEAR ON MONITOR AND BE PRINTED BY PRINTER.

PROCEDURE	OBSERVATION
12) REMOVE TEST TAPE, TURN POWER TO C.P.U. "OFF", REMOVE TEST CARTRIDGE, DISCONNECT ALL CONNECTIONS, CATAGORIZE C.P.U. i.e. PASS/FAIL.	

K. BYRNE

APPROVED

APPENDIX B. FUNCTIONAL SUB-BLOCK DESCRIPTION

Note: Reference Board Assemblies and Schematics for component identification.

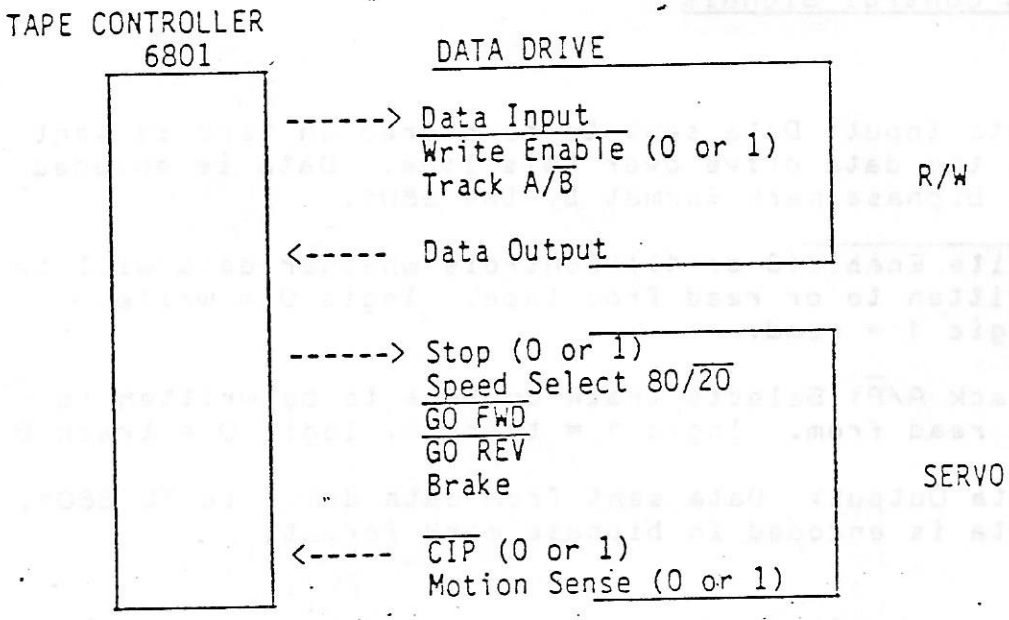
1. MASTER 6801 - "U6"

All of the operations of the AdamNet communication network are controlled by the Master 6801. The Master 6801 receives commands from the Z80, the Central Processing Unit (CPU) of the Adam Computer System. (The Z80 is located on a separate game board.) The Master 6801 communicates (receives commands) from the Z80 through 64K DRAM; it communicates with up to 15 peripheral devices through the AdamNet communication network. Commands stored by the Z80 and data taken out of 64K DRAM are relayed by the Master 6801 to the peripheral devices via AdamNet. In turn, these devices return information via AdamNet and the 64K DRAM to be read by the Z80.

2. TAPE CONTROLLER 6801 - "U24"

The Tape Controller (TC) 6801 responds to instructions received from the Z80 via the Master 6801 and functions as the commanding operator of all data drive operations. In the read/write operation, the TC 6801 generates control signals; in the data transfer and Servo operations, it controls and monitors the motion of the tape. The data and control signals (shown in Figure 1 and described below) are sent from the TC 6801 to the data drive. These signals are generated to provide data and to control the read/write (R/W) and motion (Servo) operations of the tape drive. The (0 or 1) noted means that there are two separate and distinct signals provided for drives 0 and 1, respectively.

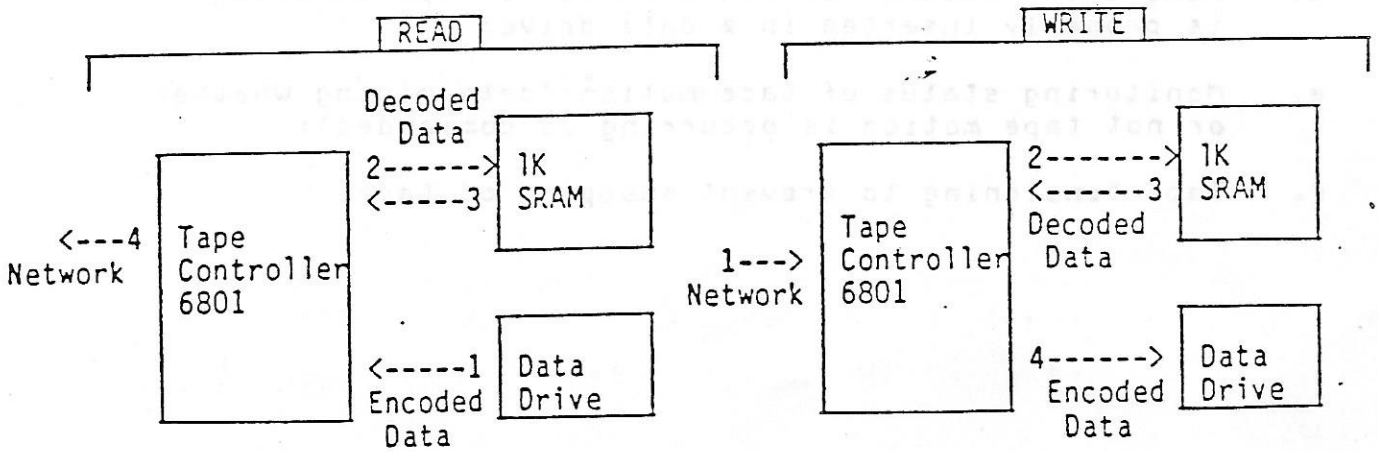
Figure 1. Data Drive Control Signals



A. READ/WRITE OPERATION

The TC 6801 is utilized twice in each read/write operation, which is limited to 1K of data at all times. (See Figure 2.) For a read operation, data must first be decoded from the biphase-mark format and transferred from the data drive to 1K static RAM. The data is then transferred from 1K static RAM to the network. For a write operation, data is first transferred from the network to 1K static RAM. The data is then encoded in biphase-mark format and transferred to the data drive for storage.

Figure 2. Biphase Mark Read/Write Decode and Encode Operation



Read/Write Data & Control Signals

1. Data Input: Data sent to be stored on tape is sent to the data drive over this line. Data is encoded in biphase mark format by the 6801.

2. $\overline{\text{Write Enable}}$(0 or 1): Controls whether data will be written to or read from tape. logic 0 = write, logic 1 = read.

3. Track A/$\overline{\text{B}}$: Selects track on tape to be written to or read from. logic 1 = track A, logic 0 = track B

4. Data Output: Data sent from data drive to TC 6801. Data is encoded in biphase mark format.

B. SERVO OPERATIONS

1. The control of all tape motion (servo) operations includes:

   a. Direction of tape motion (forward/reverse);

   b. Speed of tape motion: fast search speed = 80 inches per second, slow R/W speed = 20 inches per second;

   c. "Braking" tape motion (halting motion in milliseconds and preventing the tape from coasting to a stop);

   d. Monitoring whether or not a cassette tape cartridge is properly inserted in a data drive;

   e. Monitoring status of tape motion (determining whether or not tape motion is occurring as commanded);

   f. Tape tensioning to prevent snapping of tape.

2. Servo & Data Control Signals

a. Stop: (0 or 1) A logic 1 prevents tape motion; a logic 0 allows tape motion and enables data output. The stop lines to both drives can be a logic 1 simultaneously; but both drives cannot be in motion at the same time. Therefore, when one line is a logic 0, the other must be a logic 1.

b. $\overline{\text{Go FWD}}$: When used in conjunction with "stop" signal, logic 0 allows tape to move forward, logic 1 prevents tape from forward motion.

c. $\overline{\text{Go REV}}$: When used in conjunction with "stop" signal, logic 0 allows tape to reverse motion, logic 1 prevents reverse motion.

d. $\overline{\text{Go FWD}}$ and $\overline{\text{Go REV}}$: will not be 0 simultaneously.

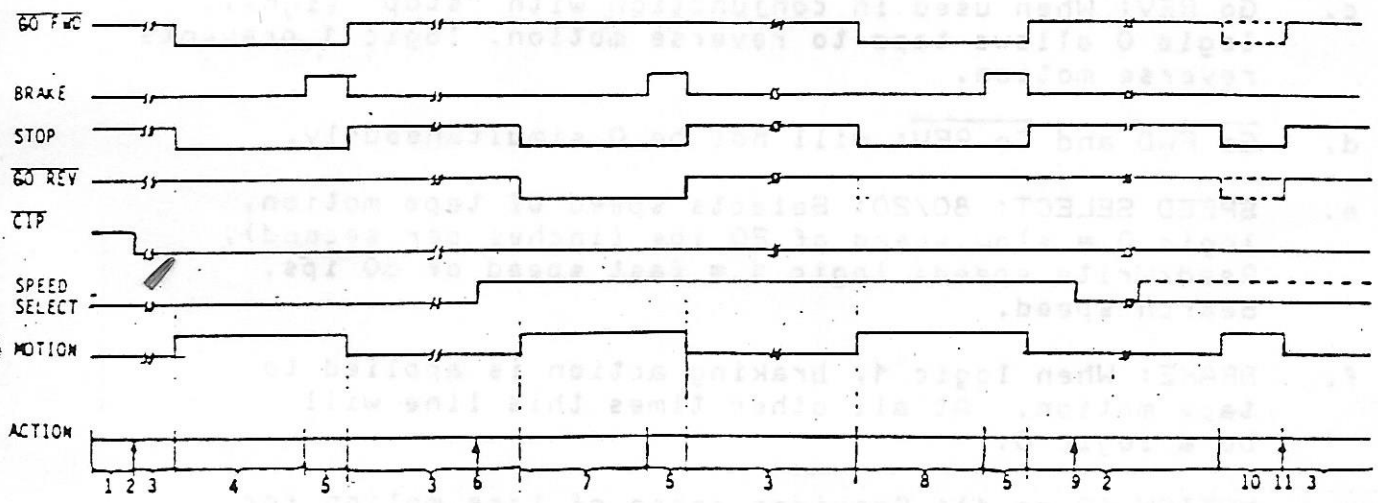
e. SPEED SELECT: 80/20: Selects speed of tape motion. logic 0 = slow speed of 20 ips (inches per second), Read/Write speed; logic 1 = fast speed of 80 ips, Search speed.

f. BRAKE: When logic 1, braking action is applied to tape motion. At all other times this line will be a logic 0.

g. MOTION (0 or 1): Provides sense of tape motion for processor. When logic 1, tape is moving properly. When logic 0, tape is not moving due to stop/braking action or malfunction of drive (jam-up, broken tape, etc.).

h. $\overline{\text{CIP}}$(0 or 1): "Cassette In Place" indicator.
logic 0 indicates tape drive has tape cartridge inserted properly;
logic 1 indicates tape cartridge is not inserted in drive.

Figure 3 - Functional Timing Diagram of the Servo Operation



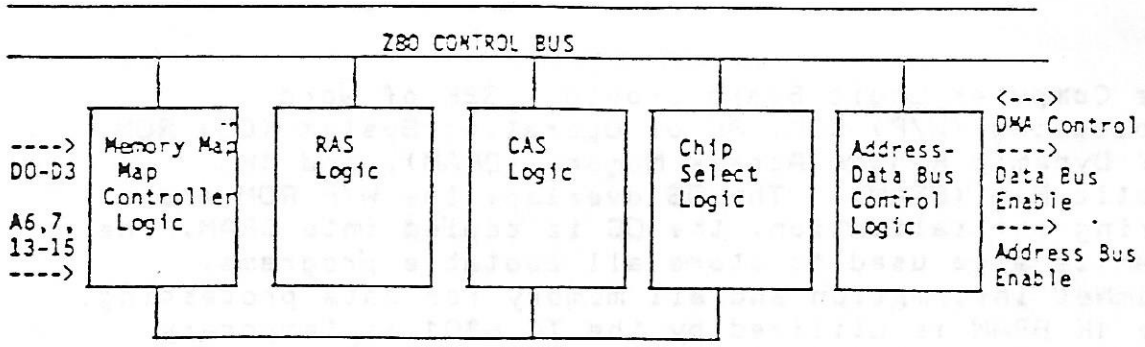
ACTION CODES

1. No motion; cassette not in place
2. Cassette placed in drive.
3. Cassette in place; no motion
4. Go forward command asserted; tape moves forward at 20 ips
5. Brake command asserted; tape motion slows down to a stop, Brake command must be removed when 'motion' line falls to logic zero.
6. 80 ips command asserted; no motion
7. Go reverse command asserted; tape moves reverse at 80 ips
8. Go forward command asserted; tape moves fast forward at 80 ips
9. 20 ips command asserted; no motion
10. FWD or REV command asserted; 80 or 20 ips
11. Tape stall/jam/drive malfunction 'motion' line falls to zero during motion command assertion without braking command asserted. All motion commands must be immediately removed until problem is fixed.

3. MEMORY INPUT/OUTPUT CONTROLLER (MIOC) (U7)

A. The MIOC performs decoding and timing for the 6801 CPU to ensure proper communication between the two microprocessors, RAM and ROM. The MIOC generates Row Address Strobe (RAS), Column Address Strobe (CAS), and Multiplex (MUX) signals for 128K of DRAM; it also provides chip selects for the operating system ROMS and auxiliary ROM and arbitrates DMA requests into 64K of DRAM. MIOC is shown functioning in the Adam System in Figure 4.

Figure 4. MIOC Functional Diagram



B. Upon power up, by default, the memory map in the MIOC directs the Z80 to 32K ROM and 32K RAM for initialization. Following initialization, the Z80 may alter the memory map depending on conditions and data received by writing to the MIOC. The Memory Map is shown in Figure 5.

C. MIOC performs housekeeping of the system with the use of RAS, MUX, and CAS signals. For example, due to the use of dynamic RAM, each bit is stored as an electric charge that needs to be refreshed every few milliseconds. To stimulate the electronic charge, RAS signals are used to read through memory, refreshing each memory bit. This operation is essential to maintain the contents of the dynamic memory. However, the contents can still be destroyed under certain conditions:

1. Prolonged reset > 1ms
2. Prolonged wait state operation > 1ms
3. Prolonged network acknowledge (DMA) > 1ms

4. MEMORY

A. The Computer Logic Board provides 32K of Word Processing (W/P) ROM, 8K of Operating System (OS) ROM, 64K Dynamic Random Access Memory (DRAM), and 1K Static Ram (SRAM). The OS overlaps the W/P ROM and during initialization, the OS is copied into DRAM. The DRAM is also used to store all bootable programs, AdamNet information and all memory for data processing. The 1K SRAM is utilized by the TC 6801 as temporary storage for all data transfers to/from the data drive.

1. W/P ROM: U20, U22.
2. OS ROM: U21.
3. DRAM: U11 - U18.
4. SRAM: U26, U27.

B. Connectors are provided on the Computer Logic Board for optional expansion on.board capabilities: these include a Modem, 64K DRAM and 32K ROM.

5. INTERCONNECT TO Z80 SYSTEM

A. The Computer Logic Board is designed to interface with both the Delta Game Board and the ColecoVision Board. Two different interconnects are required to mate the Computer Logic Board with the two Z80 system boards; both are described below.

1. Interconnect to Delta Game Board (used in Delta Module).

   This interconnect, which consists of two 30-pin ribbon cables, a dual 30-pin card edge connector and a small PCB, makes a pin-for-pin connection between J1 on the Computer Logic Board and J2 on the Delta Game Board.

2. Interconnect to ColecoVision Board (used in Exp.Mod.#3).

   This interconnect, which consists of two 30 pin ribbon cables, a dual 30-pin card edge connector, and a buffer board, makes the connection between J1 on the Computer Logic Board and the expansion port of the ColecoVision Unit. Many of the connections are made pin-for-pin between the two boards. The exceptions to this are listed below:

   a. A0-A15: These lines are buffered. The input to the buffer is from the ColecoVision and tristate control of the buffer (ADDRBUFEN) is from the Computer Logic Board.

   b. D0-D7: These lines are buffered bidirectionally. The RD signal from the ColecoVision controls the direction (when active, data flows toward the ColecoVision) and the 245EN signal controls the tristate function.

   c. $\overline{\text{IORQ}}$: This line is connected directly between the two boards (pin 55) and is also buffered (controlled by ADDRBUFEN) and connected to pin 40 of the Computer Logic Board.

   d. O' Clock: This line, pin 40 of the ColecoVision, is connected to pin 45 of the Computer Logic Board.

Interconnect to ColecoVision Board Continued...

e. Ø Clock: This line, pin 45 of ColecoVision, is not connected.

f. $\overline{M1}$, $\overline{MREQ}$, RFSH, WR, $\overline{RD}$: These lines are buffered. The input to the buffer is from the ColecoVision, and the tristate control of the buffer (ADDRBUFEN) is from the Computer Logic Board.

6. THE Z80 SYSTEM

A. The Z80 CPU, located on the Delta Game Board and the ColecoVision Board, is the controlling CPU of the Adam Computer System. The Z80 CPU system will initialize in one of two modes, dependent of which reset switch has been activated: the game mode or the computer mode. The mode of operation is determined by the memory map shown in Figure 5. The Z80 is capable of configuring the memory map into any combination of lower and upper memory and switching between them. In order to use 64K DRAM, the Z80 sends I/O commands through MIOC, which selects the required memory map option.

Figure 5. Memory Map

	Computer Mode OPTIONS			Game Mode
64K DRAM	1	2	3	4
Lower 32K Choices	32K Boot ROM	32K RAM1	32K RAM2 (SLOT)	8K ColecoVision Operating System 24K RAM1
Upper 32K Choices	32K RAM1	32K AUX ROM (SLOT)	32K RAM2 (SLOT)	32K EXT. ROM GAME CARTRIDGE

B. An M1 wait request hardware is included that enables the Z80 to automatically introduce one clock period to the memory fetch cycle. Memory timing requirements are as follows.

1. Operating System & W/P ROM

   a. Access time from chip select to data output valid ... 300 ns max.

   b. Access time from Output Enable to Data Valid ... 150 ns.

   c. Access time from Address Valid to Data Valid ... 450 ns.

2. DRAM

   a. Access time from Row Address Strobe (RAS) ... 250 ns max.

   b. Access time from Column Address Strobe (CAS) ... 165 ns max.

APPENDIX C. ANNOTATED LOGIC BOARD SCHEMATIC

Reference schematic 41843 Rev E4

Circuit Node		Comment
A	+5V	
B	+12V Inductive	
C	+12V Logic	
D	-5V	
E	$\overline{\text{PBRST}}$	Active low with computer reset switch.
F	$\overline{\text{RST}}$	Master 6801 and Z80 reset from MIOC.
G	$\overline{\text{NET}}$ $\overline{\text{RST}}$	Adam Net reset from MIOC.
H	B0	3.58 MHz Z80/MIOC Clock.
I	D0 - D7	Date Buss "Active".
J	A0 - A15	Address Buss "Active".

APPENDIX D. LOGIC BOARD TEST WITH GAMMA DEBUG CARTRIDGE

1. The Gamma D-Bug Rev. 2 cartridge is to be inserted into the game connector on a known working Delta for testing both the Delta logic board or the Gamma logic board. The Delta logic board or Gamma logic board to be tested is connected to the board. A TV or monitor should be connected to the game board. See Appendix E for additional trouble- shooting hints.

   a. Turn the power on. Use game reset switch. If the screen never showed information after a game reset use TABLE I (in Appendix E) to troubleshoot the problem.

   b. If MENU gets displayed, press button #1 on hand controller 1. If faults are displayed (an X on the screen), narrow the cause of the faults by using Check Sum Test with ROMs on the logic board. Compare the results of the checksum #4 and test #1 with TABLE II. If there are no faults but BA15 does not have a blinking check mark see TABLE II; 11, 13, (BA15 must blink to indicate the board passes the test).

   NOTE: BA15 will not be tested if there are any faults on the screen. The space next to BA15 may remain blank.

   c. The message "PRESS * TO TEST CELLS" will appear in the lower left of the screen if there is a blinking BA15 check mark. At this time the board can be flexed or heat or cold can be directed to the board to test for intermittent problems. Faults will be displayed.

   d. Press the * on controller 1 to enter the RAM cell test. The RAM cell blanks the screen for a few seconds. If a bad cell is detected in memory locations less than 8000H the display and test will freeze after displaying the chips that could not be written to or read from properly. If all of the chips are faulty see TABLE II, 10. If even one chip passes then the chips with faults should be replaced to eliminate the fault.

e. All the RAM chips pass this test, only if the check mark next to U18 blinks every several seconds consistantly as the test continues to cycle.

f. Use game reset to escape.

g. Press button #4 on hand controller 1 to do a checksum test. The ROMs should be in the logic board for this test. U2 is the game board ROM and it should equal D483. If an incorrect check sum is displayed for any ROM see TABLE II; 11, 12, 14. If a check sum is done without ROMs on the logic board, U2 must equal D483 and the others must change as a finger is moved along the edge connector on the logic board. ROMs do not need to be installed to run Gamma Debug (independent of WP Rev level). It is recommended to put ROMs on the board if no faults show up using any test on this cartridge but the board fails final testing (see note above). If ROMs with more than 64K memory are inserted in positions U8, U20, U21, U22 the check sum displayed will not agree with the check sum on the chip (record the "half" check sum displayed from a known good board and use that sum).

ROM CheckSum listing

System Rev level	Checksums			
77	CEC1,	ACE8,	A463,	0C95
80	DC0E,	AEB9,	B113,	F385

APPENDIX E

COLECO INDUSTRIES, INC.

TEST PROCEDURES

PROCEDURE NO: TP-008-A

DATE: October 25, 1983

SUBJECT: Adam Logic Board Testing with Gamma D Bug Cartridge

1.0 SCOPE

This troubleshooting technique is performed using the Gamma D Bug Game Cartridge, a known good Delta game board, AND this test procedure. Charts are available in the procedure to help narrow faults down quickly. The cartridge doesn't depend on the logic board RAM for operation. There are only a few signals that could have problems that would keep the cartridge from working. These signals are listed in a chart. This cartridge will pick out and display almost any problem that can occur to the address bus, data bus, RAM or RAM control signals and ROM or ROM control signals. The cartridge does not test through the AdamNet and therefore does not test the tape circuitry. All 512K RAM cells are tested to determine if they can be toggled high and low. ROM is tested by performing a check sum on each chip and displaying it. Special wave forms are generated for the address bus and data bus that simplify using an oscilliscope to view these lines.

NOTE: This cartridge will not test lines through the AdamNet. The tape control section is not tested. The 6801 chips can remain active for Tests #1, #4 and #5.

2.0 EQUIPMENT NEEDED

2.1 Gamma D Bug Cartridge Rev. 2

2.2 Oscilloscope

2.3 Known Good Delta Game Board

2.4 Television

2.5 Power Supply for Game Board & Logic Board

3.0 APPLICABLE DOCUMENTS

3.1 Logic Board Schematic #41843

3.2 P.I. Report #106 Method Of Test

PREPARED BY:	APPROVAL:	SUPERCEDES:
B. Taylor	Lee Hamed 11/21/83	TP-008

5.0 VIEWING SIGNALS ON AN OSCILLOSCOPE Continued

Next with the probe on BA14 adjust the scope to see just two pulses on the scope (Figure 1,D). This will show a little more than one complete program cycle. Look for more than one distinct level near ground. Two different levels indicate a probable short to another line. For BA3 to BA0 there will be a pulse once per program cycle that shows as both high and low.

Be sure to put the probe on each chip that may be suspected and "read" the signal at the pin of the chip.

If button #2 is depressed while resetting the game board, RA7 should show 6 high pulses between each program cycle (Figure 1,C). If these extra pulses are not there then the BRFSH signals are not getting through. Look at BRFSH, BM1, BA6 and Ø signals for proper activity and logic levels. If button #2 on the controller is not depressed at the time of a game reset, the six extra high pulses per cycle may or may not show when viewing RA7. Continously reset the game board and press button #2 until the six pulses do not show up. If they always show up look at BRFSH, BM1, BA6 and Ø for proper signals.

5.4 Press game board reset.

5.5 Press button #3 on controller 1 (DATA LINES).

5.6 A binary count signal should be seen on the scope when looking at the data lines. It is not necessary to trigger on pin 20 of the Z80 but it might be useful to make a clearer display on the scope (refer to Figure 2)

5.7 Press game board reset.

5.8 Press button #5 on controller 1 (PINS 19 & 20 of U7).

5.9 A 50% duty cycle square wave should be seen on pins 19 and 20 of U7. If the signal is there but is more like 30%/70% on either output then the signal on pin 11 of U7 is low when it shouldn't be or U7 is faulty (also see table II, 8, 14).

4.0 AUTOMATIC TESTS Continued

4.7 Press button #4 on hand controller 1 to do a check sum test. The ROMs should be in the logic board for this test. U2 is the game board ROM and it should equal D483. If an incorrect check sum is displayed for any ROM see TABLE II, 11, 12, 14. If a check sum is done without ROMs on the logic board U2 must equal 0483 and the others must change as a finger is moved along the edge connector on the logic board. It is recommended to put ROMs on the board if no faults show up using any test on this cartridge but the board fails final testing (see note above). If ROMs with more than 64K memory are inserted in positions U8, U20, U21, U22 the check sum displayed will not agree with the check sum on the chip (record the "half" check sum displayed from a known good board and use that sum).

5.0 VIEWING SIGNALS ON AN OSCILLOSCOPE

The 6801 (U6) should have its crystal shunted, or remove the 6801 for best viewing of signals.

5.1 Reset game board.

5.2 Press button #2 on controller 1 (ADDRESS LINES).

5.3 It is not essential that a second probe be connected to pin 20 of the Z80 but it might be useful to make a clearer display on the scope. A binary count will be seen when probing the address lines except for BA15, BA3, BA2, BA1, BA0 and maybe RA7. BA14 through BA4 will have an easy signal to look at. BA14 will have a pulse train twice as long as BA13 which will have a pulse train twice as long as BA12 etc. to BA4. Remember BA7 and RA7 are different signals. RA7 may have extra high pulses per cycle. BA3 to BA0 also have fairly clean signals that can be looked at for opens or shorts.

Signals BA14, BA13, BA12, BA11, BA10, BA9, BA8, BA7, BA6, BA5 and BA4 should be looked at for a normal binary count (Figure 1,E,F,G). Two lines shorted will show the same activity and it will be apparent that at least one seems "out of order" in the binary count. BA15 should always be active (Figure 1,D).

4.0 AUTOMATIC TESTS

The Gamma D Bug Rev. 2 cartridge is to be inserted into the game connector on a known working Delta game board for testing both the Delta logic board or the Gamma logic board. The Delta logic board or Gamma logic board to be tested is connected to the game board. A TV or monitor should be connected to the game board.

4.1 Turn the power on. Use game reset switch. If the screen never showed information after a game reset use TABLE I to trouble-shoot the problem.

4.2 If the MENU gets displayed, press button #1 on hand controller 1. If faults are displayed (an X on the screen), narrow the cause of the faults down by using the Check Sum test with ROMs on the logic board. Compare the results of the Check Sum test #4 and test #1 with TABLE II. If there are no faults but BA15 does not have a blinking check mark see TABLE II, 11, 13,(BA15 must blink to indicate the board passes the test).

✳ NOTE: BA15 will not be tested if there are any faults on the screen. The space next to BA15 may remain blank.

4.3 The message "PRESS * TO TEST CELLS" will appear in the lower left of the screen if there is a blinking BA15 check mark. At this time the board can be flexed or heat or cold can be directed to the board to test for intermittent problems. Faults will be displayed.

4.4 Press the * on controller 1 to enter the RAM cell test. The RAM cell test blanks the screen for a few seconds. If a bad cell is detected in memory locations less the 8000H the display and test will freeze after displaying the chips that could not be written to or read from properly. If all of the chips are faulty see TABLE II, 10. If even one chip passes then the chips with faults should be replaced to eliminate the fault.

4.5 All the RAM chips pass this test, only if the check mark next to U18 blinks every several seconds consistantly as the test continues to cycle.

4.6 Use game reset to escape.

6.0 NOTES:

6.1 If there is a fault on the output side of multiplexers U9 or U10 there will be two (2) BA errors displayed associated with the MA error displayed (see figure 3). (An exception is MA7 will only cause RA7 to show a fault while BA15 remains untested - blank).

6.2 If there is a fault on the input side of the multiplexers U9 or U10 there will be one (1) BA error displayed associated with the MA error displayed.

6.3 If every time test #1 is selected BD error(s) are displayed and BA and MA conditions are displayed (not blank) then RAM has been written to and read from successfully at location 2000H. This means that the data buss probably has no problems. RAM is outputing wrong data at other locations. If the symptoms can not be found in Table II then the fault is probably a bad RAM chip. There should be an X in the appropriate MA column indicating the faulty chip.

6.4 All errors for test #1 are determined by writing to RAM and analyzing what is read back. So all symptoms are related to what is read from RAM.

TABLE I

MENU DOESN"T COME UP

Look at Z80A (U1)

PIN #	NAME	NORMAL SIGNAL
20	IORQ	Active
18	HALT	Always high
17	NMI	Always high
16	INT	Always high with 6801 (U6) not on board or 6801 (U6) cyrstal shorted OR Active with 6801 (U6) operating
6	ϕ	50% Duty Cycle 3.5 mHz
23	Busak	Same as pin 16 (INT) on Z80A
24	WAIT	Active
25	BUSRQ	Same as pin 16 (INT) on Z80A
29	RESET	Goes low for either reset OR Always high after reset (PBRST pin 25 U7 and CVRST pin 6 U7 must be high)

Look at Custom Chip (U7)

PIN #	NAME	NORMAL SIGNAL
3	BA15	Active(a short low or open can blank screen)
4	BA14	Low after reset a short high freezes screen
5	BA13	Active a short high freezes screen
17	DMA	Same as pin 16 (INT) ON Z80A
14	IORQ	Active
22	AUXDECODE 1	Active (a low will freeze screen)
27	ADDBUFEN	Same as pin 16 (INT) on Z80A
29	245EN	Always high for menu - could be low if BA15 is high

Look at ColecoVision Chip U7 (LS05)

PIN #	NAME	NORMAL SIGNAL
5	AUXDECODE 2	Always high

COLECO INDUSTRIES, INC.

TEST PROCEDURES

PROCEDURE NO: TP-008-A

DATE: October 25, 1983

SUBJECT: Adam Logic board Testing w/Gamma 0 bug Cartridge

TABLE II

SIGNALS TO OR FROM U7

DISPLAY SYMPTOMS

1. All DB0- DB7 Non Flashing errors, no BA or MA test (blank)

NAME	PROBLEM LEVEL	NOTES
BA15	High	Check sum U2 & U8=D483;U20,21,22= Wrong
BA13	Low	Check Sums okay
ADDBUFEN	High	Check Sum U2 & U8=D483; U20,21,22= Wrong
BMREQ	High	Check Sum U2 & U8=D483; U20,21,22= Wrong
BWR	High	
245EN	High	Check Sum U2 & U8=D483; U20,21,22= Wrong
CAS1	Low	Check Sum U2=D483; others are blank

2. All BA0-BA15 & MA0-MA7 Non Changing errors, no BD errors

BA6	Low	Check Sum U2 & U8=D483; U20,21,22= Wrong
BA7	High	" " " " " " " "
SUXDECODE1	High	Check Sum okay
IOREQ	High	Check Sums all Wrong

3. All BA0-BA15 errors, maybe some BD errors, changing MA errors, some chips have all MA0-MA7 errors (with PROMs in typically U12, U14, U15, U16 have all MA errors)

BM 1	Low	Check Sum okay
BRFSH	Low	Might reset to menu or stop blinking
B0	Low or high	Check Sum okay
RAS	Low or high	Check Sum okay
BRD	High	Check Sum U2=D483; U8,U20,21,22= Wrong
CAS1	High	Check Sum okay
MREQ	Low	Check Sum okay

4. BA0-RA7 All errors & MA0-MA7 errors, no BD errors

MUX	High

5. BA8-BA15 All errors & All MA0-MA7 errors, no BD errors

MUX	Low

TABLE II Continued

6. Random errors, BD or BA or MA changing

NAME	PROBLEM LEVEL	NOTES
BRFSH	Open	Usually U12,14,15,16 have all MA errors proms in. All DB errors flashing - no proms in.
BO	Open	Same as above
RAS	Open	Same as above
BRD	Open	Same as above
CAS1	Open	Same as above
BM1	Open	Same as above

7. Scattered consistant errors

BM1	Low	

8. All BD errors, All BA errors, All MA errors, no cycling (nothing blinks), Check Sum U2=D483; U8,20,21,22= Wrong

BDO	Open	Also for test #5 no pulses will be seen on pin 20 of U7 @ 10 ms/div

9. All data lines good but no BA or MA test, Check Sum U2=D483; U8,U20,21,22= Blank

BD2	Open	
DB3	Open	

10. All cells show errors, Check Sums good

BD2	Floating High	
BD3	Floating High	

!!. No BD or MA errors but Ba15 isn't blinking and can't do cell test

BA7	Open or Low	U2 & U8=D483; U20,21,22= Wrong
BOOTROMCS	Low	Check Sums okay

12. No BD or BA or MA errors, BA15 is blinking but Check Sums incorrect

BOOTROMCS	High	Check Sum for all = Wrong
BD1	Open or Low	Also will cause incorrect duty cycle on pins 19 or 20 of U7 for test #5

TABLE II Continued

13. Screen cycles while holding button * pressed through BD & BA & MA

NAME	PROBLEM LEVEL	NOTES
WAIT	High	
BA7	Open	Eventual loss of control Check Sum for U22=Wrong

14. No errors until the * is pressed, then BA15 and MA7 error. Check Sum for U2 is Wrong.

BD1	Open	Also for test #5 no pulses will be seen on pin 19 of U7 @10ms/div

15. All BD errors, All BA errors, All MA errors, but screen is cycling (blinking).

BA7	High	Check Sum U2 & U8=D483;U20,21,22= Wrong

16. Loss of control after menu is displayed.

BA7	Low	Check Sum U2=D483;U8,20,21,22= Wrong

17. Everything passes cartridge tests but fails final test.

BRSH	High	
BM1	High	These lines shorted high will not show faults but can effect computer performance.

NOTE: Signals listed in this chart may have faults and not show the same symptoms listed here. There is a form in this procedure that should be used to mark down unusual symptoms and list the cause(s). Copies should be made for other troubleshooters.

SYMPTOMS FORM

LINE CONDITIONS

			U11	U12	U13	U14
B00/	BA 0/	MA0	/	/	/	/
B01/	BA 1/	MA1	/	/	/	/
B02/	BA 2/	MA2	/	/	/	/
B03/	BA 3/	MA3	/	/	/	/
B04/	BA 4/	MA4	/	/	/	/
B05/	BA 5/	MA5	/	/	/	/
B06/	BA 6/	MA6	/	/	/	/
B07/	RA 7/	MA7	/	/	/	/
	BA 8/					
	BA 9/		U15	U16	U17	U18
	BA10/	MA0	/	/	/	/
	BA11/	MA1	/	/	/	/
	BA12/	MA2	/	/	/	/
	BA13/	MA3	/	/	/	/
	BA14/	MA4	/	/	/	/
	BA15/	MA5	/	/	/	/
		MA6	/	/	/	/
		MA7	/	/	/	/

LINE CONDITIONS

			U11	U12	U13	U14
BA0/	BA 0/	MA0	/	/	/	/
B01/	BA 1/	MA1	/	/	/	/
B02/	BA 2/	MA2	/	/	/	/
B03/	BA 3/	MA3	/	/	/	/
B04/	BA 4/	MA4	/	/	/	/
B05/	BA 5/	MA5	/	/	/	/
B06/	BA 6/	MA6	/	/	/	/
B07/	RA 7/	MA7	/	/	/	/
	BA 8/					
	BA 9/		U15	U16	U17	U18
	BA10/	MA0	/	/	/	/
	BA11/	MA1	/	/	/	/
	BA12/	MA2	/	/	/	/
	BA13/	MA3	/	/	/	/
	BA14/	MA4	/	/	/	/
	BA15/	MA5	/	/	/	/
		MA6	/	/	/	/
		MA7	/	/	/	/

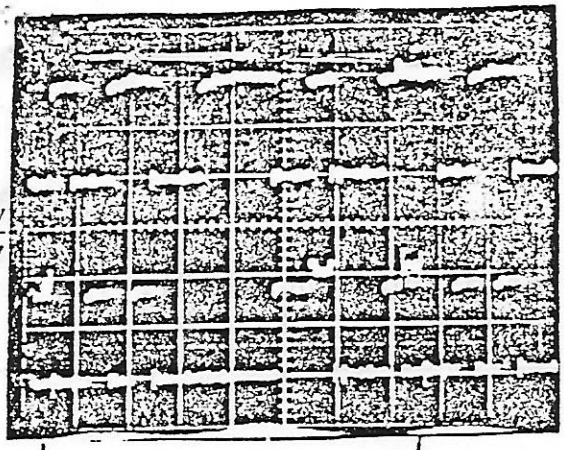
LINE CONDITIONS

			U11	U12	U13	U14
B00/	BA 0/	MA0	/	/	/	/
B01/	BA 1/	MA1	/	/	/	/
B02/	BA 2/	MA2	/	/	/	/
B03/	BA 3/	MA3	/	/	/	/
B04/	BA 4/	MA4	/	/	/	/
B05/	BA 5/	MA5	/	/	/	/
B06/	BA 6/	MA6	/	/	/	/
B07/	RA 7/	MA7	/	/	/	/
	BA 8/					
	BA 9/		U15	U16	U17	U18
	BA10/	MA0	/	/	/	/
	BA11/	MA1	/	/	/	/
	BA12/	MA2	/	/	/	/
	BA13/	MA3	/	/	/	/
	BA14/	MA4	/	/	/	/
	BA15/	MA5	/	/	/	/
		MA6	/	/	/	/
		MA7	/	/	/	/

LINE CONDITIONS

			U11	U12	U13	U14
B00/	BA 0/	MA0	/	/	/	/
B01/	BA 1/	MA1	/	/	/	/
B02/	BA 2/	MA2	/	/	/	/
B03/	BA 3/	MA3	/	/	/	/
B04/	BA 4/	MA4	/	/	/	/
B05/	BA 5/	MA5	/	/	/	/
B06/	BA 6/	MA6	/	/	/	/
B07/	RA 7/	MA7	/	/	/	/
	BA 8/					
	BA 9/		U15	U16	U17	U18
	BA10/	MA0	/	/	/	/
	BA11/	MA1	/	/	/	/
	BA12/	MA2	/	/	/	/
	BA13/	MA3	/	/	/	/
	BA14/	MA4	/	/	/	/
	BA15/	MA5	/	/	/	/
		MA6	/	/	/	/
		MA7	/	/	/	/

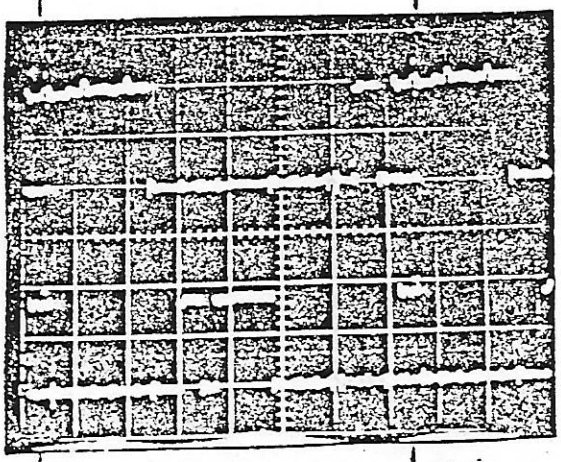
Test #2
Address Signals



2V div

A.

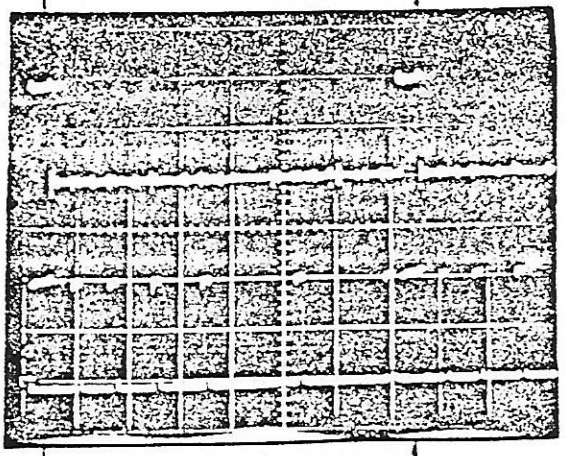
One Program cycle 2us/div



2V div

B.

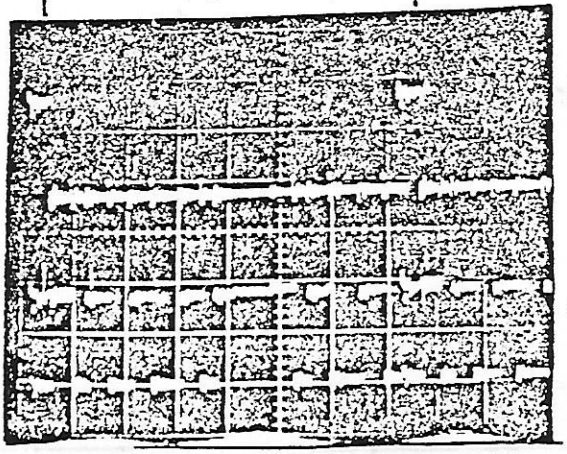
One Program cycle 2us/div



2V div

C.

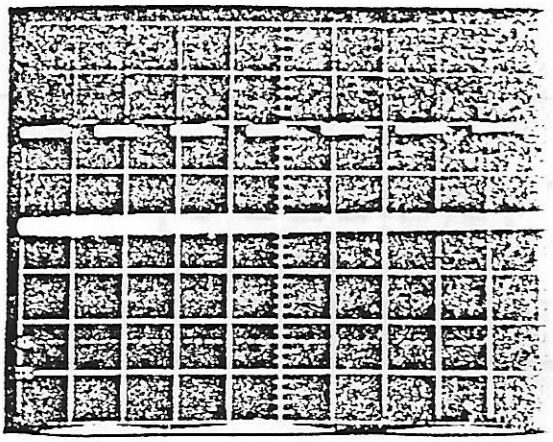
One Program cycle 2us/div



2V div

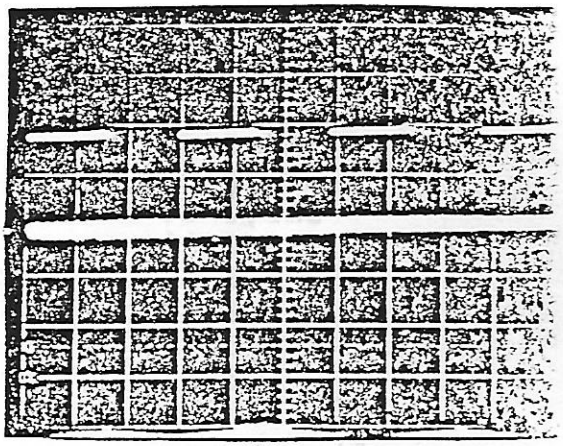
D.

2us/div



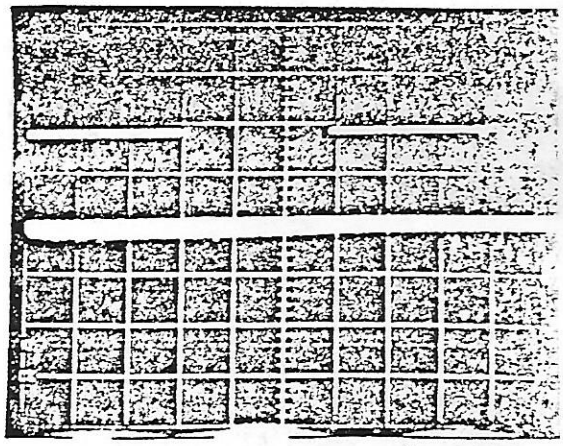
E.

5ms/div



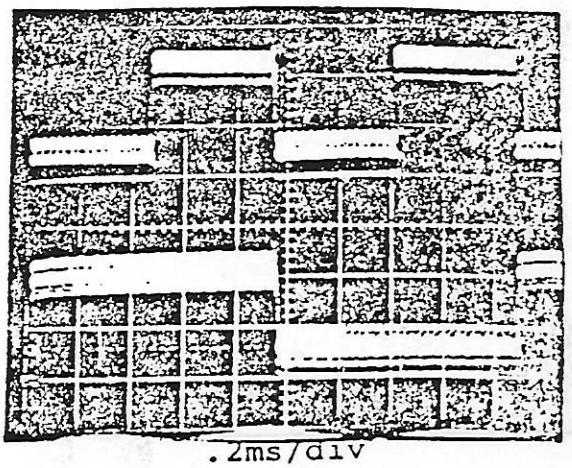
F.

5ms/div



G.

5ms/div



.2ms/div

Figure 2 Test #3 Data Signa

COLECO INDUSTRIES, INC.
TEST PROCEDURES

PROCEDURE NO: TP-008
DATE: October 25, 1983
SUBJECT: Adam Logic Board Testing w/Gamma D Bug Cartridge

INPUT		OUTPUT
BA0, BA8	mux	MA0
BA1, BA9		MA1
BA2, BA10		MA2
BA3, BA11		MA3
BA4, BA12		MA4
BA5, BA13		MA5
BA6, BA14		MA6
RA7, BA15		MA7

FIGURE 3

A fault on the output of the Mux. will cause the two adjacent BA lines to show a fault. (An exception is MA7 will only cause RA7 to show a fault while BA15 remains untested - blank).

TO: G. BUICKUS
FROM: K.BYRNE
DATE: 1/21/85 ASSEMBLY LEVEL:E4[illegible]
SUBJECT: DELTA LOGIC PCB LEVEL SYSTEM TEST PROCEDURE LOG NO.: 1[illegible]

PROCEDURE FOR CONNECTION OF LOGIC BD, SLAVE DRIVE, DRIVE SIMULATOR, SLAVE KEYBOARD, AND SLAVE PRINTER.
ENSURE THAT POWER SWITCH IS IN THE OFF POSITION!!

1) SLIDE BOARD UNDER TEST INTO EDGE CARD CONNECTOR ON FIXTURE UNTIL IT "CLICKS".

2) CONNECT ALLIGATOR CLIP TO GROUND SHIELD ON BOARD UNDER TEST. (ANY PART OF BOARD WITHOUT GREEN MASKING).

3) CONNECT 9 PIN "D" CONNECTOR LOCATED ON BREAK-AWAY PCB INTO THE 9 PIN RECEPTACLE LOCATED ON RIGHT SIDE OF FIXTURE. ENSURE THAT PRINTER IS PLUGGED INTO FIXTURE.

4) CONNECT TEST MODULE AUX.-NET CONNECTOR INTO THE LONGER OF THE TWO CABLES CONNECTED TO THE BOARD UNDER TEST.

5) CONNECT SLAVE KEYBOARD INTO THE SHORTER OF THE TWO CABLES CONNECTED TO THE BOARD UNDER TEST.

6) PLUG RIBBON CONNECTOR FROM BOARD UNDER TEST INTO EDGE CARD CONNECTOR LOCATED ON THE DELTA GAME BOARD.

7) ENSURE TEST CARTRIDGE IS INSERTED IN PORT OF THE DELTA GAME BOARD MOUNTED ON FRONT OF FIXTURE.

PROCEDURE	OBSERVATION
NOTE: BEFORE STARTING TEST ENSURE THAT THERE IS NOT A TAPE IN DRIVE.	
1) TURN POWER "ON".	1a) "ADAM ELECTRONIC TYPEWRITER" SCREEN WILL APPEAR ON MONITOR.
NOTE: 1'S MAY APPEAR ON SCREEN AND PRINTER WILL PRINT SAME.	
2) TURN POWER "OFF".	
3) CONNECT SLAVE DRIVE AND DRIVE SIMULATOR (BALL ON TOP) INTO 4 PIN RECEPTACLES ON BOARD UNDER TEST.	
4) TURN POWER "ON".	
5) INSERT "BASIC" TAPE IN SLAVE DRIVE, CLOSE DOOR.	
6) PRESS "CARTRIDGE" RESET. (LOCATED ON DELTA GAME BD).	6a) THE MESSAGE " STATION I.D." WILL APPEAR ON MONITOR.

PROCEDURE	OBSERVATION
7) TYPE IN YOUR STATION I.D. (OR PRESS RETURN)	7a) MENU SCREEN WILL APPEAR.
8) CHOOSE #2	8a) MESSAGE"ADAM OR EXPANSION" WILL APPEAR ON MONITOR.
9) TYPE "A" IF YOU ARE TESTING AN ADAM C.P.U.	9a) TAPE WILL START TO WIND.
	b) WORDS "TEST IN PROGRESS" APPEAR ON MONITOR CHECK FOR ALTERNATING COLORS OF THE WORDS.
	c) AT THE END OF 2 1/2 MIN. THE FOLLOWING WILL APPEAR ON MONITOR IF SYSTEM IS GOOD, COLOR BARS AS FOLLOWS: WHITE GREY LIGHT YELLOW DARK YELLOW CYAN (AQUA) LIGHT GREEN MEDIUM GREEN DARK GREEN VIOLET LIGHT RED MEDIUM RED DARK RED LIGHT BLUE DARK BLUE THEN AUDIO TONES WILL BE HEARD FOLLOWED BY A "CRASH" A GRID PATTERN WILL THEN APPEAR ON SCREEN, CHECK FOR UNIFORMITY OF GRID PATTERN. A SEQUENCE OF MUSICAL NOTES WILL BE HEARD FOLLOWED BY A PROMPT MESSAGE TO "TYPE IN YOUR INITIALS"ON A BACKGROUND OF WHITE. PRESS RETURN.

NOTE: TYPE IN INITIALS WHEN WHITE SCREEN APPEARS ONLY. TEST WILL RECYCLE UNTIL OPERATOR TYPES IN INITIALS.

PROCEDURE	OBSERVATION
	d) IF SYSTEM HAS FAILED SCREEN WILL FLASH RED AND WHITE WITH AUDIO
	e) IF UNIT PASSES STEP C THE MESSAGE "PASSED MANUFACTURING TEST" WILL APPEAR ON MONITOR AND BE PRINTED BY PRINTER.
10) REMOVE TEST TAPE, TURN POWER "OFF" UNPLUG 9 PIN "D" CONNECTOR, AUX AND KEYBD CONNECTORS, ALSO UNPLUG RIBBON CABLE FROM EDGE CARD CONNECTOR ON DELTA GAME BOARD. SLIDE LOGIC BOARD UNDER TEST AWAY FROM EDGE CARD CONNECTOR ON FIXTURE UNTIL BOARD CLEARS FIXTURE	

K. BYRNE

APPROVAL